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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10085009	03/01/2002	438	129	~~2812~~ 2818	Q. Hoang

**APPLICANTS: Fukui Masahiro; Hayashi Naoki;

**CONTINUING DATA VERIFIED: NONE mj

** FOREIGN APPLICATIONS VERIFIED: YES mj

JAPAN 2001-063491 03/07/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☑ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☑ yes ☐ no	60188-156
Verified and Acknowledged Examiners's intials	MM	

TITLE : Wiring method in layout design of semiconductor integrated circuit, semiconductor integrated circuit and functional macro

U.S.DEPT. OF COMM./PAT.& TM.-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING		
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg.	Print Fig.
		Primary Examiner			
☐ TERMINAL DISCLAMER		PREPARED FOR ISSUE	Applicati n Examiner		

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